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(12) # EUROPEAN PATENT APPLICATION

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(54) **Programmable die identification circuits.**

(57) An identification section fabricated onto a semiconductor chip includes memory for use in preserving die-specific information that characterizes that particular semiconductor chip. The chip may also include programmable circuitry for use in programming the die-specific information into the memory.

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The present invention generally relates to systems for preserving information relating to semiconductor chips and, more particularly, systems for preserving information regarding the manufacturing history of semiconductor chips.

Semiconductor chips, hereinafter referred to as die, are batch fabricated on wafers of semiconductor material generally five or six inches in diameter, each wafer containing a two-dimensional array of die. These wafers are processed in groups which are referred to as fabrication lots. The wafers in a given lot are numbered sequentially, and this wafer number, along with a unique fabrication lot number, are inscribed on the wafer in an area outside the array of die. Thus, during the initial fabrication process, each die may be uniquely identified by certain die-specific information such as its fabrication lot number, its wafer number, and its location within the array of die hereinafter referred to as its die position number.

The unique identification of the die serves important functions in the analysis of regular production die (e.g., the analysis of die returned by customers) and of non-production or developmental die (e.g., die characterization, reliability testing). Engineers frequently need to characterize the die by analyzing the effect of a processing variable on the electrical properties of the die. To do this, the engineer will typically split a lot into groups of wafers during fabrication, each group to be processed with the particular processing variable set to a different value. After the die are processed and individually packaged, electrical parameters of each die are tested, and the test results are saved along with its wafer number and die position number. With this data an engineer is able to compare the performance of the groups of wafers with one another, and thus determine the effect of the processing variable on die performance. This information also enables an engineer to analyze the electrical performance of the die as a function of its position on the wafer during fabrication.

The unique identification of a die serves a similar purpose in the reliability testing of the die. To test its reliability, the die may be subjected to conditions such as extreme temperatures or humidity for extended periods and then electrically tested. The unique identification of each die enables an engineer to analyze the test results and determine the reliability of the die as a function of processing parameters, and also as a function of its position on the wafer during fabrication.

The fabrication lot number also serves an important function in the analysis of defective die returned by customers. The die from a particular lot may be sold to many different customers over a long period of time. When defective die from a particular fabrication lot are returned by a customer, an engineer will typically analyze the returned die to determine the cause of the malfunction. If the engineer knows which fabrication lot the die came from, he may be able to avoid repetitive analysis on future customer returns from that same lot.

Currently, those skilled in the art view the retention of the unique identification of a die throughout the life of the die as a time-consuming, expensive, and error-prone process. In the course of normal production, the wafer number and die position number are lost after the wafer is sawed into individual die. A new assembly lot number is assigned to the lot and encoded onto each package into which the die was assembled. The fabrication lot number is retained only in the paper records for that assembly lot. Thus, an engineer faced with a die returned from a customer must search the assembly lot records for the fabrication lot number. These records are often misplaced or incomplete and are disposed of after a certain period of time. Without the information from these records, an engineer will not be able to determine which fabrication lot the die came from.

In order to retain the unique identification of each die for purposes such as die characterization or reliability testing, the wafers are sent to a non-production assembly area with special instructions to preserve the identification of each die, typically by handwriting the information on each individual package into which the die are assembled. This process is not automated, and it is very likely that the die will be mixed up and identified incorrectly. Because there is no way to ensure that the die are identified correctly, confidence in the die characterization or reliability testing is diminished greatly.

From the foregoing it can be seen that it would be quite desirable to ensure that the unique identification of each die is recorded correctly and retained throughout the life of the die. It may also be seen that it is a shortcoming and deficiency of the prior art that heretofore no system or method for accomplishing this has been developed.

To overcome the shortcomings and deficiencies of the prior art, we provide a device having a die characterized by die-specific information, where the die includes an integrated circuit and an identification section. The identification section includes a memory section for storing information and a means for programming the die-specific information into the memory section. In one aspect of the present invention, the memory section may comprise a non-volatile memory. Additionally, the non-volatile memory may be fuse-programmable.

In certain embodiments, the programming is enabled by forcing the integrated circuit into a test mode. In addition, the means for programming may further include device pins which serve other functions when the integrated circuit is not in a test mode.

The identification section of the die may further include means for reading the die-specific information from the storage means, where the reading

means may be electrically connected to the storage means. In embodiments, the reading may be enabled by forcing the integrated circuit into a test mode. In addition, the means for reading may further include device pins which serve other functions when the integrated circuit is not in a test mode.

In certain embodiments, the die-specific information may include the fabrication lot number, the wafer number, and the die position number associated with the particular die.

We also provide a method of preserving die-specific information by providing the die with a means for storing information and then programming the manufacturing information into the storage means. In certain embodiments of the-method, the storage means may comprise a non-volatile memory which in some embodiments may be fuse-programmable.

The manufacturing information may be programmed into the storage means by forcing the integrated circuit into a test mode. In addition, the die-specific information may be programmed via device pins which perform other functions when the integrated circuit is not in a test mode.

In certain embodiments, the method for preserving die-specific information may further comprise the step of electronically reading the die-specific information from the means of storing information. Further, the die-specific information may be electronically read by forcing the integrated circuit into a test mode. Still further, the die-specific information may be read via device pins which may perform other functions when the integrated circuit is not in a test mode.

In certain embodiments, the step of programming said die-specific information is accomplished during wafer sort testing, and may be performed by an automated test program.

We also provide a method for conducting engineering analysis of an integrated circuit on a die characterized by die-specific information. This method includes the steps of storing the die-specific information on the die, reading the die-specific information from the die, tying the die-specific information to data relating to the integrated circuit, and sorting that data according to the die-specific information.

Furthermore, we also provide a method of tracing manufacturing history of an integrated circuit on a die. This method includes the steps of fabricating a memory onto the die, storing information relating to the manufacturing history into the memory section, and retrieving that information from the memory section.

Accordingly, we provide a storage means on a die that may be used to trace the manufacturing history of the die easily and with accuracy.

We also provide a storage means on a die which affords an inexpensive and dependable means of identification.

In the accompanying drawings, by way of example only:

FIG. **1a** is a top plan of a single wafer containing an array of die;

FIG. **1b** is an enlarged view of one of the die shown in FIG. **1a**, this FIG. **1b** showing that the die contains an identification portion according to the teachings of the present invention;

FIG. **2** is a flowchart which illustrates the steps taken in a prior art method of handling die which method includes provisions for preserving die-specific information;

FIG. **3** is a flowchart which illustrates the steps that may be taken in a die handling method that incorporates the teachings of the present invention; and

FIG. **4** is a flowchart which illustrates a method of analyzing data relating to the electrical performance of a semiconductor device according to the present invention.

Referring now to the drawings wherein depicted elements are not necessarily shown to scale, there is shown in FIG. **1a** a single wafer generally designated by reference numeral **10**, having an array of die, this array is generally designated by reference numeral **12**. The array **12** is made up of a plurality of die **14**. As may be seen in FIG. **1b**, each individual die **14** has an identification section **16** according to the teachings of the present invention as well as an integrated circuit **18**. The identification circuit **16** is designed to occupy an area on the die **14** small enough to allow for easy insertion into existing layouts but not so small as to push design rules to the point that overall device yield will be adversely affected. In the embodiment of the present invention shown in FIG. **1b**, identification section **16** comprises three sections: a memory section **20**, programming circuitry **22**, and output circuitry **24**.

The memory section **20** is used to store die-specific information which characterizes the die **14**. The memory section **20** may be, particularly in a preferred embodiment, of a non-volatile nature in order to preserve the die-specific information for the life of the die. In a preferred embodiment, the non-volatile memory section **20** may be fuse-programmable to allow retrieval of the die-specific information, even if the die **14** becomes non-functional, by visually decoding the fuses.

The programming circuitry **22** is fabricated on the die **14** and is electrically connected by conventional means to the memory section **20**. In the embodiment shown in FIG. **1b**, the programming circuitry **22** is also electrically connected to the die pads **23** which allow electrical connection to external electrical signals. The die pads **23** allow a user to instruct the programming circuitry **22** to program the die-specific information into the memory section **20**. The die pads **23** may serve other functions in the normal operation of the

integrated circuit **18**, and may be converted for use in programming the memory section **20** by forcing the integrated circuit **18** into a test mode. Such dual operation of the die pads **23** can prove valuable to those skilled in the art because it may be employed to reduce device pin count in certain applications.

The output circuitry **24** is fabricated on the die **14** and is electrically connected to the memory section **20**. The output circuitry **24** is also electrically connected to die pads **25** which allow external access via the output circuitry **24** to the information stored in the memory section **20**. The device pads **25** may serve other functions in the normal operation of the integrated circuit **18**, and may be converted for use in reading information out of the memory section **20** by forcing the integrated circuit **18** into a test mode. As with die pads **23**, the dual operation of the die pads **25** may prove valuable to those skilled in the art because it may be employed to reduce device pin count.

Based upon the foregoing, those skilled in the art should now appreciate that, in essence, the present invention comprises a memory section on a die in which die-specific information may be stored. Associated with that memory section in embodiments of the present invention may be means for moving information into the memory and means for extracting that information. These latter two means may be the above mentioned programming circuitry **22** and output circuitry **24**.

The importance of preserving die-specific information in an identification section **16** located on a die **14** can be seen by comparing the use of a prior art method of preserving the die-specific information, shown in FIG. **2**, with the use of the method taught by the present invention of preserving the die-specific information, shown in FIG. **3**. The flowchart in FIG. **2** shows steps typical of both the standard production and non-production flow of a die **14**. The die are batch-fabricated on a single wafer **10**, each wafer **10** having a two-dimensional array of die **12** (step **30**). As discussed previously in the background of the invention section, each die **14** may be uniquely identified by its fabrication lot number, its wafer number, and its die position number. Once fabrication is completed, each die **14** is electrically tested at the wafer sort step **32** while still in wafer format. After the wafer sort step **32**, the die **14** will enter either the standard production flow (designated by arrow **34**) and ultimately be distributed to a customer, or a non-production flow (designated by arrow **36**) usually for the purpose of engineering analysis.

In the standard production flow **34**, the wafers **10** are sent to production assembly (step **38**) where the wafers **10** are scribed and the die **14** separated from each other. At this point in a standard production process, the wafer number and die position number are irretrievably lost. The die **14** are assigned a unique assembly lot number and the fabrication lot number is preserved in manufacturing records for that assembly lot. The assembly lot number is encoded into a date code which is marked onto the package into which the die **14** was assembled. At the test step **40** following the production assembly step **38**, each packaged die **14** is electrically tested and units which pass the test are forwarded to a distributor (step **42**) for shipment to a customer (step **44**). If the customer determines that the packaged die is defective, it is customary for the customer to return the die to its manufacturer (shown as step **46**) for failure analysis (shown as step **48**). Failure analysis may often involve determining whether a die was misprocessed. In order to determine whether a die was misprocessed, those skilled in the art find it advantageous to know the fabrication lot from which the die **14** originated. The fabrication lot number can typically be found only in the manufacturing records for the assembly lot indicated on the device package. Because the packaged die may have remained at a distributor site for an extended period of time before shipment to the customer, by the time the die **14** is returned as defective, the manufacturing records are often lost or purged. Consequently, the manufacturer is unable to trace the die **14** back to a fabrication lot in order to determined whether the die **14** was misprocessed or not.

In a non-production flow route **36**, the die **14** are typically used by engineers for engineering analysis such as device characterization or reliability testing. As discussed previously in the background of the invention section, this engineering analysis often involves splitting a fabrication lot into groups, each group being fabricated according to different settings of processing variables. In this context, the identification of each die **14** serves an essential function of correlating a particular die **14** to a particular setting of a processing variable. Referring back again to FIG. **2** and the non-production flow route **36**, after the wafer sort step **32**, the wafers **10** are sent to local assembly (step **50**) where the workers are often instructed to preserve die-specific information such as the fabrication lot number, wafer number and die position number by handwriting the information on each package into which the die **14** is assembled. Those skilled in the art, (that is, the engineers that want to use the die for engineering analysis) view this step as expensive and exceedingly error-prone. Also, after the local assembly step **50** no means are available by which to verify the die-specific information marked on any particular package. When the packaged die are then returned to the engineers for testing (step **52**), the die-specific information for each die is manually read off the package and recorded with the test results for that die. The test data is then sorted according to the fabrication lot number, wafer number or die position number to analyze lot to lot, wafer to wafer, or position to position variation in die electrical performance, respectively. This analysis takes place at step **54** shown

in FIG. 2. If the test results deviate from what was expected, those skilled in the art will typically suspect an error in die identification and will repeat the experiment with a new fabrication lot (step 56).

The use of the identification section 16 according to the teachings of the present invention in a production and non-production flow of an integrated circuit is shown in the flowchart of FIG. 3. Each die 14 is fabricated to include a programmable identification circuit (e.g. the circuit 16 as shown in FIG. 1b). This fabrication step is shown as step 60 in FIG. 3. At the wafer sort step 62, each die 14 on the wafer 10 may be electrically connected to an automated test machine which executes a series of routines testing the electrical properties of the die 14. The test machine may also program the fabrication lot number, wafer number and die position number specific to a particular die into the identification section 16 of that die 14. To do so, the test machine may force the die 14 into a test mode and apply electrical signals to the die pads 23 connected to the programming circuit 22 such that the information is stored in the memory section 20. To eliminate the need for excess pads on the die 14, existing pads that serve other functions during normal operation of the die may be converted for use in accessing the identification section 16 when the die is in a test mode. At any time following the programming of the die-specific information, this information can be retrieved from the die 14 either electronically, by forcing the die 14 into a test mode and reading the information stored in the identification section 16, or by decapping the packaged die and visually examining the fuses in the identification section 16. Other retrieval means may also be employed.

In the standard production flow (designated by arrow 64 in FIG. 3), the die next enter the production assembly step 68. Because the die-specific information is programmed into the identification section 16 of each die 14, this information is not lost at the production assembly step 68 when the wafers 10 are scribed and the die 14 separated from each other. Following the production assembly step 68, the packaged die are electronically tested (step 70) and the die which pass the test are advanced to the distribution step (shown as step 72) for eventual shipment to a customer (step 74). If the customer returns the packaged die to the manufacturer (step 76) for failure analysis (step 78), the manufacturer will be able to trace the die back to a fabrication lot by reading the die-specific information preserved in the identification section 16 of that die 14, whether the die is functional or not.

In a non-production flow (designated by arrow 66 in FIG. 3), the die 14 are sent to local assembly (step 80) following wafer sort test (step 62). Because the die-specific information is preserved in an identification section 16 on each die 14, it is not necessary at this step 80 to manually track the die-specific information nor to handwrite the information on each package into which a die is assembled. At the following test step 82, the die-specific information may be electronically read from the die 14 and this information is stored with the test data corresponding to that die (step 84). The data may then be analyzed to determine lot to lot, wafer to wafer, or position to position variations in electrical performance of the die. The use of the identification section 16 to preserve the die-specific information allows the engineer to be confident that the die are correctly identified. If the results are not as expected, the engineer may verify the die-specific information by electronically reading the information from the packated die (step 86). Thus, the use of a programmble identification circuit according to the teachings of the present invention may allow an engineer to at least eliminate the possibility of error at the local assembly step 80 in maintaining the correct die identification.

Based on the foregoing, it should now be clear that the present invention provides an identification section on a die characterized by die-specific information that can be used to preserve the die-specific information. The identification section includes a memory section and in certain embodiments may include a means for putting information into the memory section and may also include a means for reading the information out of the memory section. The means for putting information into the memory section may be the programming circuitry 22 shown in FIG. 1b. The means for reading information out of the memory section may be the output circuitry 24 also shown in FIG. 1b.

Referring now to FIG. 4, it may be seen that the use of the identification section 16 for preserving die-specific information offers an advantageous method of analyzing data relating to the electrical performance of a die. During fabrication (shown as step 90 in FIG. 4), each die 14 is provided with a programmable identification section 16. The die-specific information (which may include the fabrication lot number, wafer number, and die position number) is programmed into each die while still in wafer format at the wafer sort test step 92. At the device test step 94, an automated test machine performs a series of electrical tests on the device. The results of these tests are then stored in a file on disk, tape or other storage means (step 96). Also at the test step 94, the automated tester may also force the die into a test mode and thereby access the die-specific information from the memory section 20. This die-specific information is then stored on disk, tape, or other storage means and is tied to the test results for that particular die (step 96). By tying it is meant that any useful association is made with the data. At step 98, both the stored test data and the stored die-specific data are read into a post-processor for data manipulation. The test data may be sorted according to fabrication lot number,

wafer number, or die position number, or any combination thereof. The sorted test data may then be analyzed to detect lot to lot, wafer to wafer, or die position to die position variations in the electrical performance of the die.

The foregoing description shows only certain particular embodiments of the present invention. However, those skilled in the art will recognize that many modifications and variations may be made without departing substantially from the spirit and scope of the present invention. For example, the die-specific information may also include other information such as but not limited to mask revisions, test program revisions, and results of certain tests. Accordingly, within the scope of the appended claims, the present invention may be practiced otherwise than as specifically described hereinabove.

Claims

1. A device including an integrated circuit on a die characterized by die-specific information, said die comprising an identification section, said identification section comprising:
   a memory section for storing said die-specific information; and
   a means for programming said die-specific information into said memory section.

2. A device as recited in claim **1**, wherein said memory section comprises a non-volatile memory.

3. A device as recited in claim **2**, wherein said non-volatile memory comprises a fuse-programmable memory.

4. A device as recited in claim **1**, wherein said integrated circuit may be forced into a test mode, and wherein said programming means is enabled by forcing said integrated circuit into said test mode.

5. A device as recited in claim **4**, wherein said programming means comprises device pins, which device pins serve other functions when said integrated circuit is not in said test mode.

6. A device as recited in claim **1**, further comprising means for reading said die-specific information from said memory section.

7. A device as recited in claim **6**, wherein said integrated circuit may be forced into a test mode, and wherein said means for reading said die-specific information is enabled by forcing said integrated circuit into said test mode.

8. A device as recited in claim **7**, wherein said reading means comprises device pins, which device pins serve other functions when said integrated circuit is not in said test mode.

9. A device as recited in claim **1**, wherein said die-specific information comprises a fabrication lot number, said fabrication lot number identifying a fabrication lot from which said integrated circuit originated.

10. A device as recited in claim **1**, wherein said die-specific information comprises a wafer number, said wafer number identifying a wafer from which said integrated circuit originated.

11. A device as recited in claim **1**, wherein said die-specific information comprises a die position number.

12. A die characterized by die-specific information and comprising an integrated circuit and an identification section, said identification section comprising:
   a memory section for storing said die-specific information; and
   a means for programming said die-specific information into said memory section.

13. A method for preserving die-specific information characterizing a die, said die including an integrated circuit, and said method comprising the steps of:
   providing said die with a means for storing information; and
   programming said die-specific information into said means for storing information.

14. A method as recited in claim **13**, wherein said step of providing said die with a means for storing information comprises the step of providing said die with a memory section.

15. A method as recited in claim **14**, wherein said step of providing said die with a memory section comprises the step of providing said die with a non-volatile memory.

16. A method as recited in claim **15**, wherein said step of providing said die with said non-volatile memory comprises the step of providing said die with a fuse-programmable memory.

17. A method as recited in claim **13**, wherein said integrated circuit may be forced into a test mode, and wherein said step of programming said die-specific information comprises the step of forcing said integrated circuit into said test mode.

18. A method as recited in claim **17**, wherein said step of programming said die-specific information comprises the step of programming via device pins, which device pins serve other functions when said integrated circuit is not in said test mode.

19. A method as recited in claim **13**, further comprising the step of reading said die-specific information from said means for storing information.

20. A method as recited in claim **19**, wherein said integrated circuit may be forced into a test mode, and wherein said step of reading said die-specific information comprises the step of forcing said integrated circuit into said test mode.

21. A method as recited in claim **20**, wherein said step of reading said die-specific information comprises the step of reading via device pins, which device pins serve other functions when said integrated circuit is not in said test mode.

22. A method as recited in claim **13**, wherein said die originated on a wafer, wherein said wafer was subjected to a sort testing, and wherein said step of programming said die-specific information is effected during wafer sort testing.

23. A method as recited in claim **22**, wherein said wafer sort testing is effected by an automated test program, and wherein said programming of said die-specific information is performed by said automated test program.

24. A method of conducting engineering analysis of an integrated circuit on a die, said die characterized by die-specific information, said integrated circuit having data related thereto, and said method comprising the steps of:

storing said die-specific information on said die;

reading said die-specific information from said die;

tying said die-specific information to said data relating to said integrated circuit; and

sorting said data according to said die-specific information.

25. A method of tracing the manufacturing history of an integrated circuit on a die, said manufacturing history represented by die-specific information, said method comprising the steps of:

fabricating a memory section onto said die;

storing said die-specific information into said memory section; and

retrieving said die-specific information from said memory section.

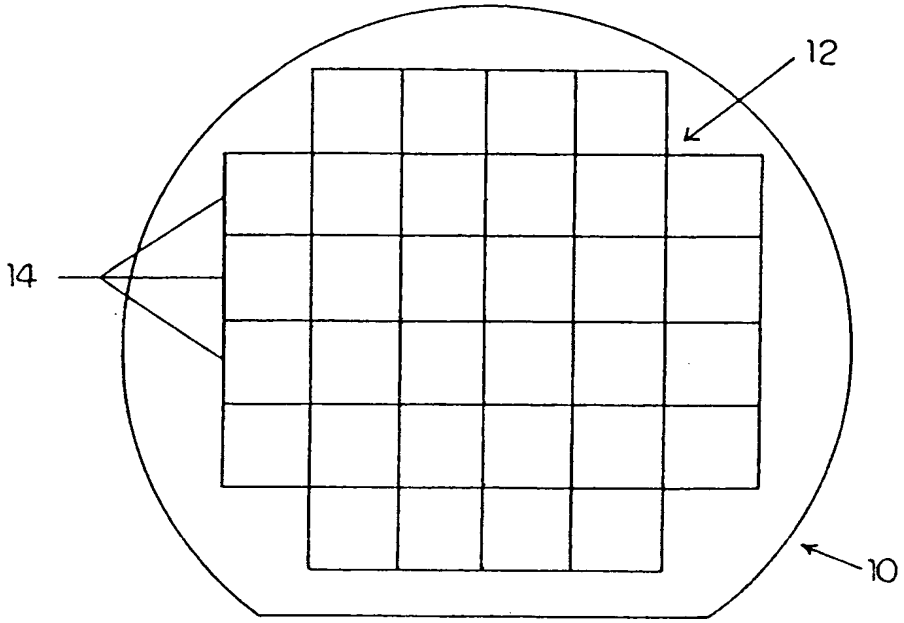
12
14
10

FIG. 1A

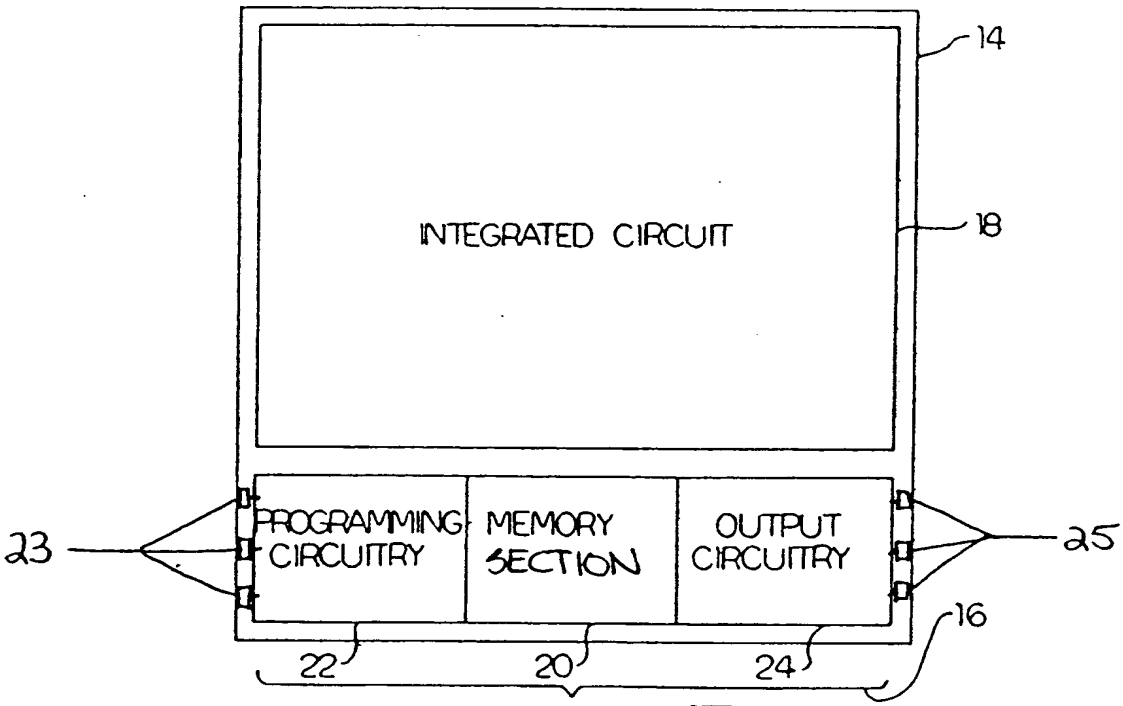
14
INTEGRATED CIRCUIT
18
PROGRAMMING CIRCUITRY
MEMORY SECTION
OUTPUT CIRCUITRY
23
25
22
20
24
16

FIG. 1B

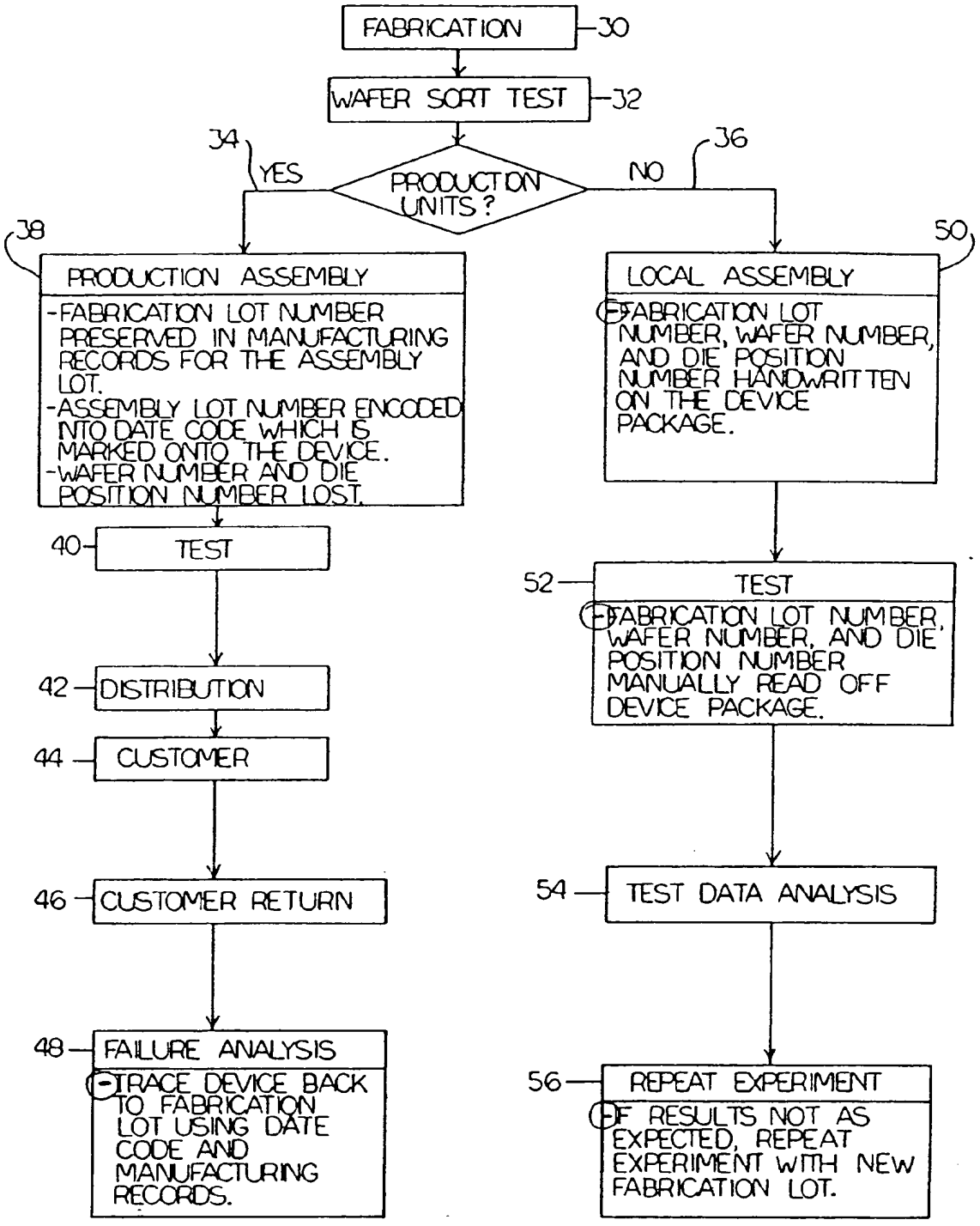

FIG. 2
(PRIOR ART)

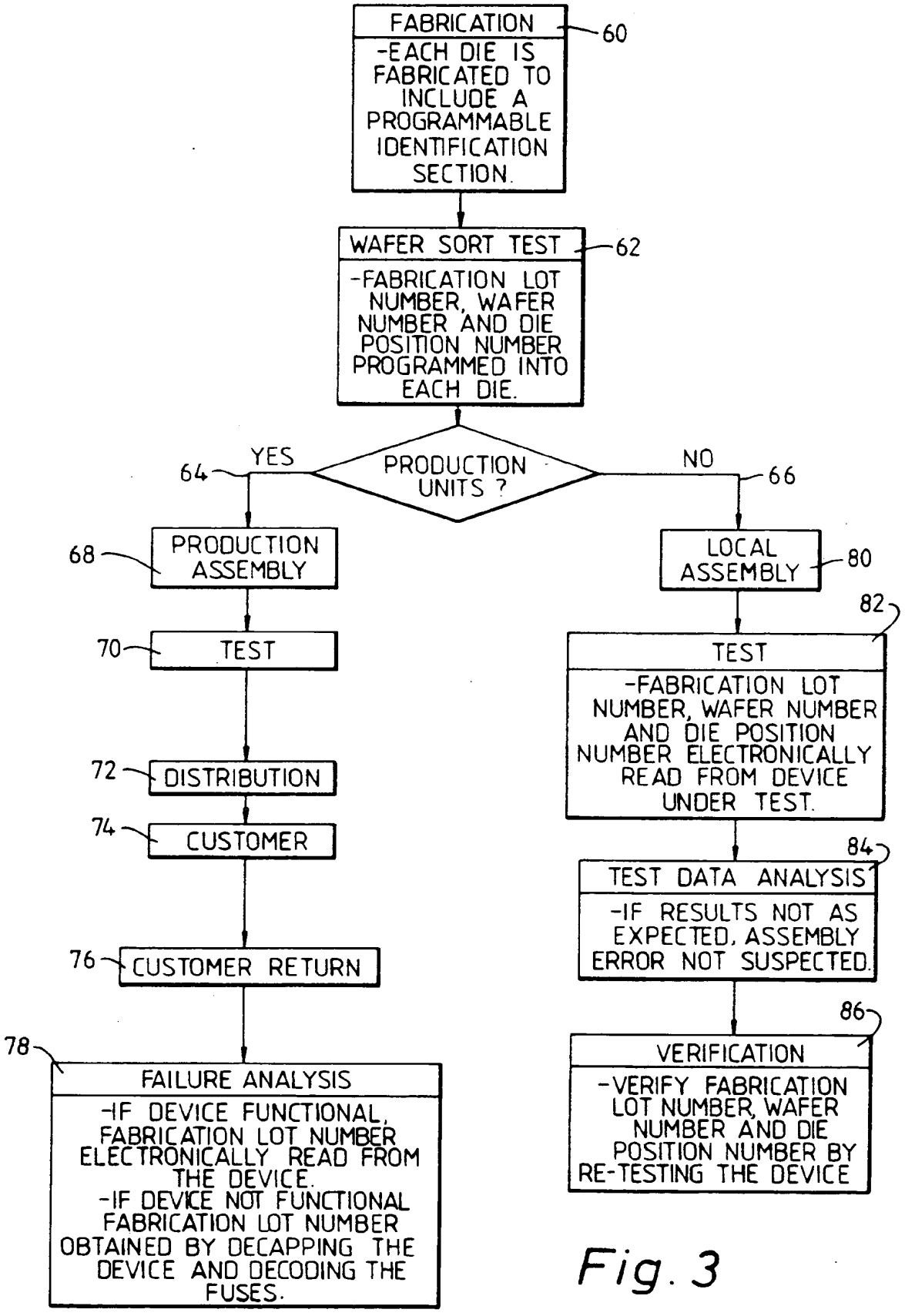
FABRICATION
-EACH DIE IS FABRICATED TO INCLUDE A PROGRAMMABLE IDENTIFICATION SECTION.
60
WAFER SORT TEST
-FABRICATION LOT NUMBER, WAFER NUMBER AND DIE POSITION NUMBER PROGRAMMED INTO EACH DIE.
62
PRODUCTION UNITS ?
YES
64
NO
66
PRODUCTION ASSEMBLY
68
TEST
70
DISTRIBUTION
72
CUSTOMER
74
CUSTOMER RETURN
76
FAILURE ANALYSIS
-IF DEVICE FUNCTIONAL, FABRICATION LOT NUMBER ELECTRONICALLY READ FROM THE DEVICE.
-IF DEVICE NOT FUNCTIONAL FABRICATION LOT NUMBER OBTAINED BY DECAPPING THE DEVICE AND DECODING THE FUSES.
78
LOCAL ASSEMBLY
80
TEST
-FABRICATION LOT NUMBER, WAFER NUMBER AND DIE POSITION NUMBER ELECTRONICALLY READ FROM DEVICE UNDER TEST.
82
TEST DATA ANALYSIS
-IF RESULTS NOT AS EXPECTED, ASSEMBLY ERROR NOT SUSPECTED.
84
VERIFICATION
-VERIFY FABRICATION LOT NUMBER, WAFER NUMBER AND DIE POSITION NUMBER BY RE-TESTING THE DEVICE
86

Fig. 3

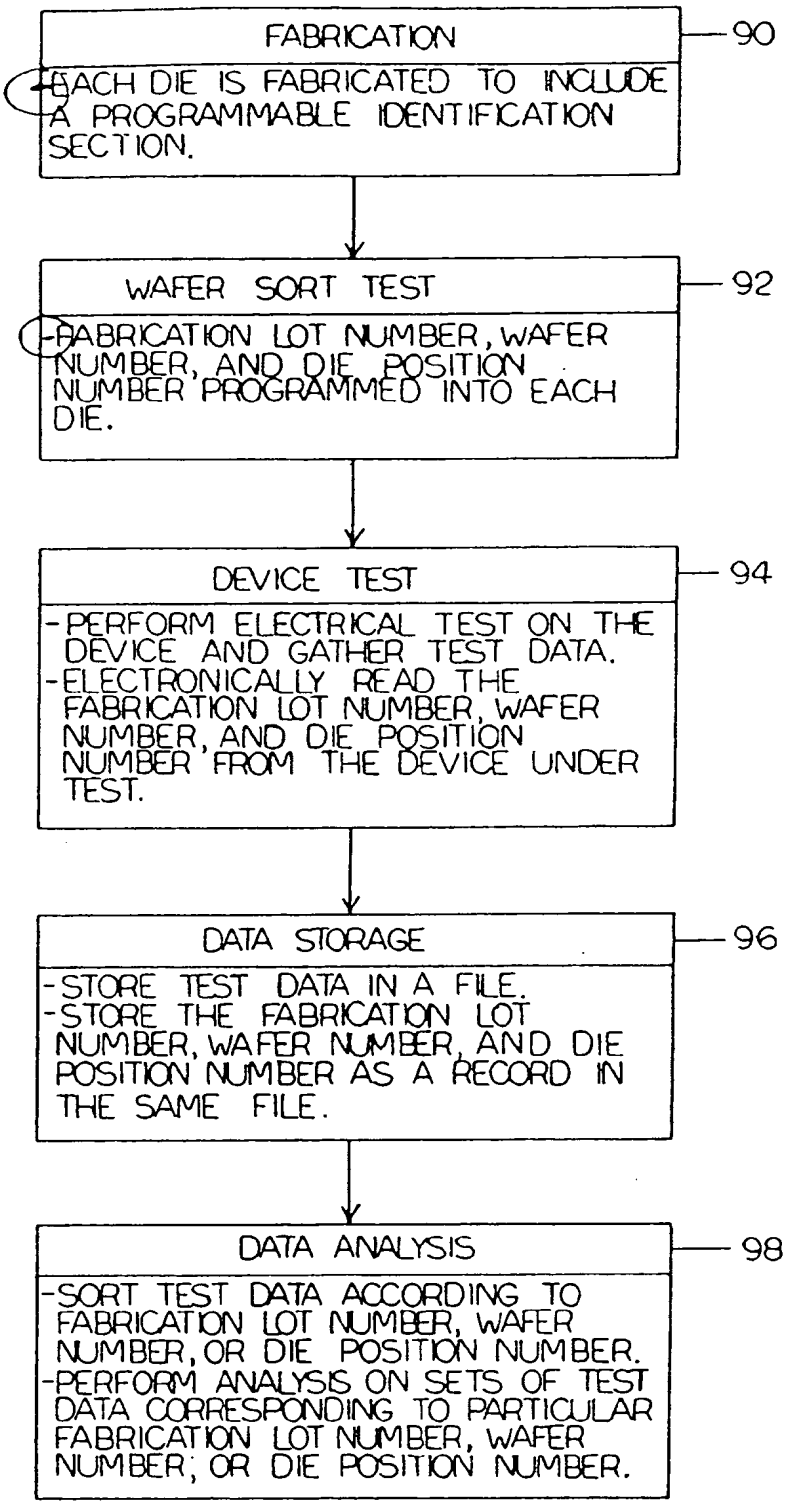
FABRICATION
90
-EACH DIE IS FABRICATED TO INCLUDE A PROGRAMMABLE IDENTIFICATION SECTION.
WAFER SORT TEST
92
-FABRICATION LOT NUMBER, WAFER NUMBER, AND DIE POSITION NUMBER PROGRAMMED INTO EACH DIE.
DEVICE TEST
94
-PERFORM ELECTRICAL TEST ON THE DEVICE AND GATHER TEST DATA.
-ELECTRONICALLY READ THE FABRICATION LOT NUMBER, WAFER NUMBER, AND DIE POSITION NUMBER FROM THE DEVICE UNDER TEST.
DATA STORAGE
96
-STORE TEST DATA IN A FILE.
-STORE THE FABRICATION LOT NUMBER, WAFER NUMBER, AND DIE POSITION NUMBER AS A RECORD IN THE SAME FILE.
DATA ANALYSIS
98
-SORT TEST DATA ACCORDING TO FABRICATION LOT NUMBER, WAFER NUMBER, OR DIE POSITION NUMBER.
-PERFORM ANALYSIS ON SETS OF TEST DATA CORRESPONDING TO PARTICULAR FABRICATION LOT NUMBER, WAFER NUMBER, OR DIE POSITION NUMBER.

FIG. 4

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(54) Programmable die identification circuits.

(57) An identification section fabricated onto a semiconductor chip includes memory for use in preserving die-specific information that characterizes that particular semiconductor chip. The chip may also include programmable circuitry for use in programming the die-specific information into the memory.

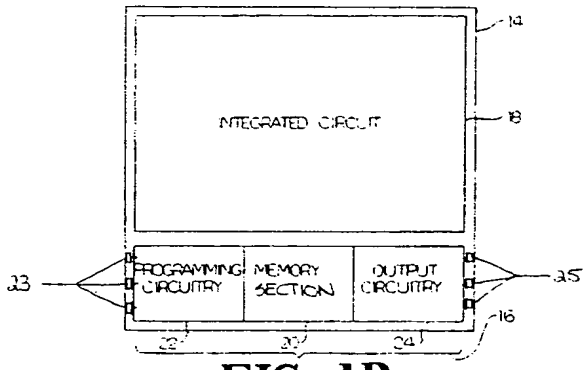

FIG. 1B

EP 0 578 410 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 30 4980

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	IBM TECHNICAL DISCLOSURE BULLETIN, vol.22, no.5, October 1979 pages 1879 - 1880 'array chip identification' * the whole document * ---	1-4,6	G06F11/00 H01L23/544
X	EP-A-0 132 520 (INTERNATIONAL BUSINESS MACHINES) * abstract * * page 4, line 15 - page 6, line 28 * * page 7, line 12 - page 8, line 5 * * page 9, line 30 - page 10, line 21 * * page 12, line 13 - page 13, line 26 * ---	1,2,6, 10-13, 22-24	
X	PATENT ABSTRACTS OF JAPAN vol. 8, no. 285 (E-287) (1722) 26 December 1984 & JP-A-59 150 464 (TOSHIBA) 28 August 1984 * abstract * ---	1,2,9,25	
X	IBM TECHNICAL DISCLOSURE BULLETIN, vol.23, no.5, October 1980 page 1829 HUTCHINS 'semiconductor chip traceability method' * the whole document * ---	1,2,9, 13,25	TECHNICAL FIELDS SEARCHED (Int.Cl.5) G06F H01L
X	EP-A-0 430 844 (INTERNATIONAL BUSINESS MACHINES) * column 2, line 15 - line 26 * ---	1,2,5,8	
X	RESEARCH DISCLOSURE, no.308, December 1989, NEW YORK US page 954, XP000096126 'component identification data retrieval via serial interface' * the whole document * --- -/--	1,2,8	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	18 November 1994	Guivol, Y

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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& : member of the same patent family, corresponding document

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Application Number
EP 93 30 4980

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	EP-A-0 057 645 (FAIRCHILD CAMERA & INSTRUMENT) * abstract; figure 2 *	1-3	
X	US-A-4 451 903 (JORDAN) * abstract * * column 1, line 59 - column 2, line 27 * * column 3, line 34 - line 49 * * column 5, line 8 - line 39 *	1,2,5,6, 8,13-15	
X	US-A-4 055 802 (PANOUSIS) * the whole document *	1-3, 13-16,18	
X	GB-A-2 244 339 (SAMSUNG) * abstract *	1-3,5,6, 8	
A	EP-A-0 420 388 (SGS-THOMSON) * abstract *	4	TECHNICAL FIELDS SEARCHED (Int.Cl.5)
X	EP-A-0 353 530 (SIEMENS) * the whole document *	1,2,4	

The present search report has been drawn up for all claims

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